# System of Numeration

## System of Numeration Conversion

**Table 1:** *Conversion between two different base numbers.*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | **Binary** | **Octal** | **Decimal** | **Hexadecimal** |
| **Binary** |  |  |  |  |
| **Octal** |  |  |  |  |
| **Decimal** | Division by 2 rule | Division by 8 rule |  | Division by 16 rule |
| **Hexa-decimal** |  |  |  |  |

**Note that:**

1. **Table 1** shows the way to convert a number at base of row to number at base of column.
2. ,,and are notations for the digit of number in Binary, Octal, Hexa-decimal, respectively.
3. See **Table 2** to converse between Binary, Octal, and Hexadecimal.

*Example:*

1110 1100 00112 EC316; 111 011 000 0112 73038

**Table 2:** *First 16 numbers in some special system of numeration.*

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Decimal** | **Binary** | **Octal** | **Hexa-**  **decimal** | **Decimal** | **Binary** | **Octal** | **Hexa-**  **decimal** |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
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# Boolean Algebra and Logic Components

## Boolean Theorems

**Table 3:** *Boolean algebra properties.*

|  |  |  |
| --- | --- | --- |
| **Property** | **AND** | **OR** |
| Commutative |  |  |
| Associative |  |  |
| Distributive |  |  |
| Identity |  |  |
| Complement |  |  |
| DeMorgan’s |  |  |
| Absorption |  |  |
| Common Identities |  |  |
| Summation |  | |

## Minterm – Maxterm

Given a function with 3 variable or . represents for -th minterm and represents for -th maxterm. Minterm and maxterm are compliment of each other, namely, or

*Example:*

## Basic Logic Components

### Basic Logic Gates

**Table 4:** *Logic gates.*

|  |  |  |  |
| --- | --- | --- | --- |
| **Gate** | **Boolean Expression** | **Logic Diagram Symbol** | **Truth Table** |
| **NOT** |  |  | |  |  | | --- | --- | |  |  | |  |  | |  |  | |
| **AND** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |
| **OR** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |

|  |  |  |  |
| --- | --- | --- | --- |
| **Gate** | **Boolean Expression** | **Logic Diagram Symbol** | **Truth Table** |
| **NAND** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |
| **NOR** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |
| **XOR** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |
| **XNOR** |  |  | |  |  |  | | --- | --- | --- | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |  |  |  | |

### Universal Gates

**Table 5:** *Universal gates.*

|  |  |  |  |
| --- | --- | --- | --- |
| **LF**([[1]](#footnote-1)) | **Logic Gates** | **NAND** | **NOR** |
| **NOT** |  |  |  |
| **AND** |  |  |  |
| **OR** |  |  |  |
| **NAND** |  |  |  |
| **NOR** |  |  |  |

|  |  |  |  |
| --- | --- | --- | --- |
| **LF** | **Logic Gates** | **NAND** | **NOR** |
| **XOR** |  | Delay 3 times | Delay 3 times |
|  |  |
| Delay 4 times | Delay 4 times |
|  |  |

# Integrated Circuit

## Adder

### Half Adder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| C:\Users\USER\AppData\Local\Microsoft\Windows\INetCache\Content.Word\800px-Half-adder.svg.png | |  |  |  |  | | --- | --- | --- | --- | | **INPUT** | | **OUTPUT** | | |  |  |  |  | |  |  |  |  | |  |  |  |  | |  |  |  |  | |  |  |  |  | |

### Full Adder

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| C:\Users\USER\AppData\Local\Microsoft\Windows\INetCache\Content.Word\550px-Full-adder.svg.png | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **INPUT** | | | **OUTPUT** | | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  | 1 | 0 | |  |  |  | 0 | 1 | |  |  |  | 0 | 1 | |  |  |  | 1 | 1 | |

## Decoder

### Decoder 2→4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | | **CONTROL** | **INPUT** | | **OUTPUT** | | | | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | |  |  |  |  |  |  |  | |

### Decoder 3→8

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | | **CONTROL** | | | **INPUT** | | | **OUTPUT** | | | | | | | | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |  |  |  |  |  |  |  |  |  |  |  |  |  |  | |

## Multiplexer (MUX)

### Mux 4→1

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | |  |  |  |  | | --- | --- | --- | --- | | **CONTROL** | **INPUT** | | **OUTPUT** | |  |  |  |  | |  |  |  |  | |  |  |  |  | |  |  |  |  | |  |  |  |  | |  |  |  |  | |

The output Y is given by

|  |  |  |
| --- | --- | --- |
|  |  |  |

Where: is the -th minterm of function 2 variables B and A.

*Example:*

### Mux 8→1

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | |  |  |  |  |  | | --- | --- | --- | --- | --- | | **CONTROL** | **INPUT** | | | **OUTPUT** | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |  |  |  |  |  | |

The output Y is given by

|  |
| --- |
|  |

Where: is the -th minterm of function 3 variables C, B, A.

*Example:*

## Logic Map for DLD

State diagram

Wave form

Truth table

Circuit

Function

K’ map

1. () LF: Logic function. [↑](#footnote-ref-1)